WHAT IS CLAIMED IS:

1. A method for transmitting a "J" bit block of data from a first electronic unit to a second electronic unit over a signaling bus having "K" signaling conductors, where zero to "K-1" of the signaling conductors is faulty, the method comprising the steps of:
identifying faulty and nonfaulty signaling conductors in the signaling bus;
setting a fault status of the signaling conductors in the first electronic unit and in the second electronic unit, using information found by the step of identifying faulty and nonfaulty signaling conductors in the signaling bus;
determining "F", the number of faulty signaling conductors in the signaling bus;
determining "K-F", the number of nonfaulty signaling conductors in the signaling bus; and
transmitting the "J" bit block of data over the "K-F" nonfaulty signaling conductors using "J/(K-F)" beats, plus an additional beat if a remainder exists.
2. The method of claim 1, the step of transmitting further comprises the steps of:
selecting a "K" bit group of data from the "J" bit block of data;
transmitting, on a beat, "K-F" bits of the "K" bit group of data, using the "K-F" nonfaulty conductors;
storing the "F" bits in the "K" bit group that cannot be transmitted, on the beat, due to the "F" faulty conductors in the signaling bus;
repeating the above three steps until all "J" bits of the "J" bit block of data have been selected; and
transmitting the stored "F" bits on one or more additional beats, using one or more of the "K-F" nonfaulty signaling conductors.
3. The method of claim 2, the step of storing the "F" bits further comprising the step of shifting at least one bit of the "F" bits into a first end of a shift register.
4. The method of claim 3, further comprising the step of transmitting at least one of the bits of the the shift register to a nonfaulty signaling conductor.

5. The method of claim 4, further comprising the step of moving a particular bit in the shift register to align that particular bit for coupling to a nonfaulty signaling conductor.

6. The method of claim 2, further comprising the steps of:
storing, in the second electronic unit, "K-F" bits per beat for "J/(K-F)" beats; and
storing remainder bits in an additional beat, if "J/(K-F)" results in a remainder.

7. The method of claim 1, further comprising the steps of:
selecting a "K-F" bit group of bits from the "J" bit block of data on the first electronic unit;
transmitting the "K-F" bit group of bits from the first electronic unit to the second electronic unit using the "K-F" nonfaulty signaling conductors in the signaling bus, using a beat of the signaling bus;
repeating the previous steps until all "K-F" bit groups have been transmitted; and
transmitting any remaining bits of the "J" bit block of data on the first electronic unit to the second electronic unit using some or all of the "K-F" nonfaulty signaling conductors, using an additional beat of the signaling bus.

8. An apparatus for transmitting a "J" bit block of data from a first electronic unit to a second electronic unit comprising:
a first block of data in the first electronic unit holding "J" bits for transmission;
storage in the second electronic capable of holding a second block of data having "J" bits;
a signaling bus having "K" signaling conductors coupling the first electronic unit to the second electronic unit, the signaling bus having "F" faulty signaling conductors and "K-F" nonfaulty signaling conductors;
a diagnostic unit coupled to the first electronic unit and to the second electronic unit capable of identifying the "F" faulty signaling conductors and the "K-F" nonfaulty signaling conductors on the signaling bus and storing fault identification information in the first electronic unit and in the second electronic unit; and

a driving sequencer in the first electronic unit that, respondent to the fault identification information, transmits the "J" bits of data using "J/(K-F)" beats, plus an additional beat if a remainder exists, using only the "K-F" nonfaulty conductors.

9. The apparatus of claim 8, the first block of data being selectable by select groups of "K" bits at a time.

10. The apparatus of claim 8, the driving sequencer capable of selecting "K-F" bits at a time from the first block of data, and driving the "K-F" selected bits onto the "K-F" nonfaulty signaling conductors of the signaling bus, the driving sequencer further capable of selecting fewer than "K-F" bits for an additional beat if "J/(K-F)" has a remainder.

11. The apparatus of claim 10, the driving sequencer further comprising drivers capable of being disabled; wherein the driving sequencer disables a driver coupled to a faulty signaling conductor.

12. The apparatus of claim 10, the second electronic unit further comprising a receiving sequencer coupled to the signaling bus and to the diagnostic unit, the receiving sequencer capable of storing "K-F" bits at a time into the second block of data, the "K-F" bits received from the "K-F" nonfaulty signaling conductors of the signaling bus, the receiving sequencer further capable of storing fewer than "K-F" bits if "J/(K-F)" has a remainder.

13. A method for transmitting a block of data from a first electronic unit to a second electronic unit over a signaling bus, comprising the steps of:
identifying nonfaulty signaling conductors in the signaling bus; and
transmitting the block of data using a transmission sequence from the first electronic unit to the second electronic unit, the transmission sequence utilizing all of the nonfaulty signaling conductors in the signaling bus;
wherein the transmission sequence uses a minimum number of beats to complete the transmission of the block of data.

14. The method of claim 13, wherein the nonfaulty signaling conductors are identified during a power on sequence.

15. The method of claim 13, wherein the nonfaulty signaling conductors are identified by a wire test performed as a result of a parity error, and error correcting code error, or a cyclical redundancy check error.

16. The method of claim 13, further comprising the steps of:

identifying a faulty signaling conductor in the signaling bus; and

switching a driver coupled to the faulty signaling conductor to a high impedance state.